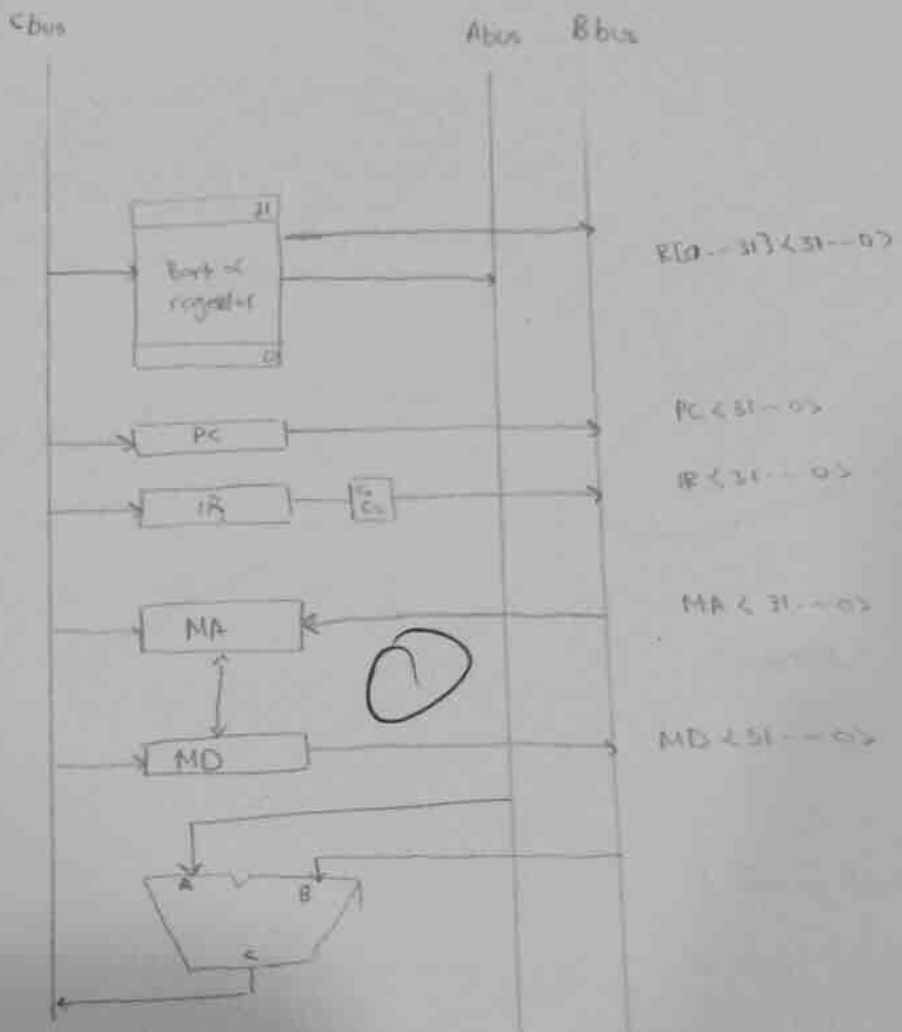
Q1:

A) Draw a complete high level architecture of a 3- Bus SRC processor. (6 marks)



5.5

B) Write the concrete RTN of the following instructions assuming 3- Bus system:

i. shc **(4 marks)**

$T_0 - T_4$ Fetch

T_5 $n \leftarrow IR\langle 4..0\rangle$

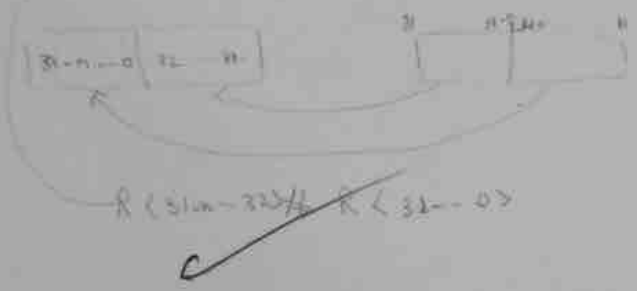
T_6 $(n=0)\ (n \leftarrow R[rc]\langle 4..0\rangle)$

T_7 $SH(i=(n\neq 0) : 0 @ R[rd]\langle 31..1\rangle \leftarrow R[rd]\langle 31..1\rangle ,\ n \leftarrow n-1 ;\ shr)$

$R\langle 32\rangle \leftarrow R\langle 32\rangle$ ~~$\leftarrow R\langle 31..1\rangle$~~

T_8 $R[rd] \leftarrow R[rd]$

* control same as Page 4



ii. st **(4 marks)**

$T_0 - T_3$ Fetch

T_4 $MD \leftarrow R[ra]$;

T_5 $MA \rightarrow (rb=0 \leftarrow 0 : rb \neq 0 \leftarrow R[rb]) : M[MA] \leftarrow MD$;

Rara , Rout , MD_{bus}

Gr_b , MA in , MD.wr

End

** Fetch instruction

T_0 $MA \leftarrow PC : PC \leftarrow PC+4 ; MD \leftarrow M[MA]$

T_1 $IR \leftarrow MD$

PCout , MD in , INC

PCin , MDrd

MDout , IR in

C) Assuming that you are using 2-Bus System:

i. Write the concrete RTN of shc instruction using the 2-Bus system assuming that the value of n is $(00101)_2$ (4 marks)

n = 5

T_0 MA ← PC — PCout ; R=B ; MAin

T_1 MD ← M[MA] ; PC ← PC + 4 — MDrd ; PCout ; PCin ; INC ; Wait

T_2 IR ← MD — MDout ; C=B ; IRin

T_3 n ← IR<4...0> — IRout ; Id

T_4 n=0 (n ← R[rc]<4...0>) — Grc ; Rout ; Id

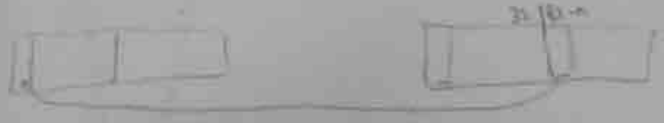
T_5 shc (n=0) : — same as purple 3

T_6 R[ra] ← R[rb] — ; n ← n-1 ; shc) ; GrB ; Rout ; shc ; Dec ; Bri Rin ; GrB ; Rout ; C=B ; GrA ; R in

CPI = 6 + 5 = 11

other

more for step T_5



R[32] ← R[11-n] ; R[11] ← R[32]

ii. Given the following delays : **(8 marks)**

Delay name	Value of the delay
Gate (Buffer) delay time	5 ns
Bus delay time	5 ns
Logic delay time	14 ns
Flip-Flop (Latch) delay	3 ns

Assuming that the worst case delay can be estimated as the maximum delay of the instructions in step T_0. Calculate the frequency of both 2-Bus and 3-Bus systems?

2-Bus

T_0 MA ← PC .

Buffer → Bus → ALU → Bus → latch

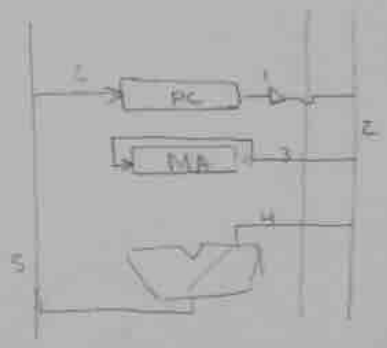
$T = d_{buf} + d_{bus} + d_{alu} + d_{bus} + d_{latch}$

$= 5 + 5 + 14 + 5 + 3 = 32$

$F = \frac{1}{T} = \frac{1}{32} = 0.03125\,ns$

3-Bus

T_0 MA ← PC : PC ← PC + 4 : MD ← M[MA]



Buffer → Bus → latch → ALU → Bus → latch

$T = d_{buf} + d_{bus} + d_{alu} + d_{alu} + d_{buf} + d_{latch}$

$= 5 + 5 + 3 + 14 + 5 + 3$

$= 35$

$F_{req} = \frac{1}{T} = \frac{1}{35} = 0.0283\,ns$

iii. **Using the information given in part A. i, and part B. i, and part B. ii, calculate the numerical speed up percentage if you are executing the instruction <u>shc</u> on a 3-Bus system over the case of executing the same instruction using a 2-Bus system?** **(8 marks)**

2bus

ET = IC * CPI * T

= 1 * 11 * 32

= 352

3-bus

ET = IC * CPI * T

= 1 * 10 * 35

= 350

+n-1

speed up = $\frac{\text{max} - \text{min}}{\text{min}} \times 100$

= $\frac{352 - 350}{350} \times 100$

= 0.57%

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* Assume IC (instruction counter) = 1

* Assume n in 3bus = (00101)
= 5

iv. **Assume that there is extra three clock cycles are required in case of using a 2-Bus system to read from the memory, recalculate part iii using this assumption? (8 marks)**

CPI in 2bus = 11 + 3 more = 14

2-bus

ET = IC * CPI * T

= 1 * 14 * 32

= 448

3bus

ET = IC * CPI * T

= 1 * 10 * 35

= 350

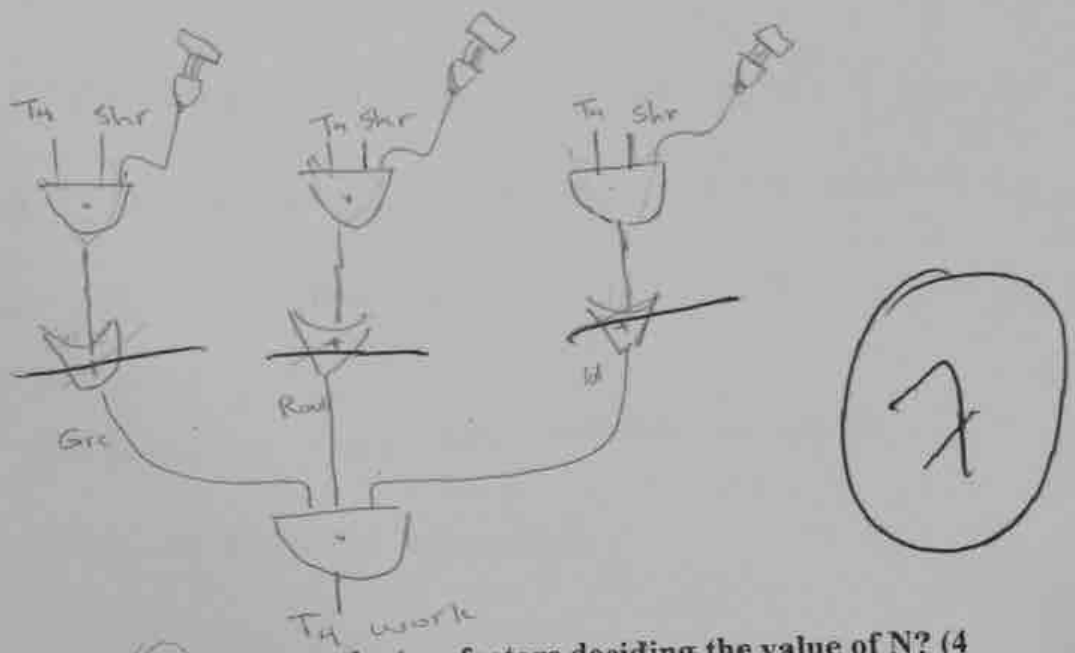
$$\text{Speed UP} = \frac{\text{max} - \text{min}}{\text{min}} \times 100$$

$$= \frac{448 - 350}{350} \times 100 = 28\%$$

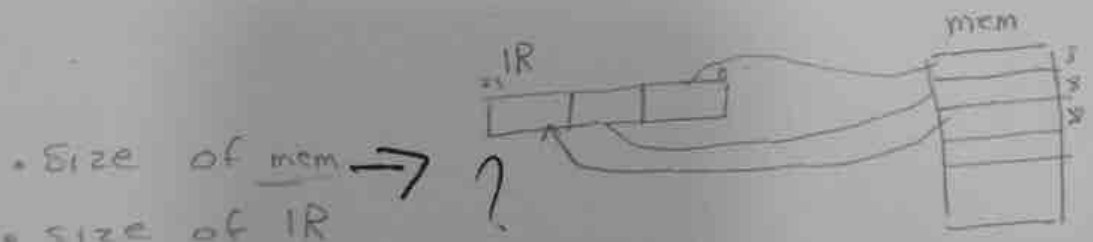
Q2: **Answer the following questions:**

i. **Implement the control signals Grc, Rout, and Ld in the following step of shr operation using 1-Bus system. Assume all required logic gates. (8 marks)**

	Instruction	Control Signals
T_4	n≠0 → (n← R[rc]<4...0>);	n≠0 →(Grc, Rout, Ld)



ii. **The instruction PC ← PC+N, what are the two factors deciding the value of N? (4 marks)**



iii. Assume that we do not have the bank of register in the 1-Bus system. Discuss if this may be cause any problem or not? (6 marks)

bank of register is Cache memory

- the speed of CPU is very very high and the speed of memory is slow if CPU match speed of memory (don't use the bank of register) this will slow down the processor

So we use the cache to solve this problem we should use hierarchy (step by step) to communicate

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